CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A method of fabricating a thin vertical channel (FIN) metal oxide semiconductor field effect transistor (MOSFET) comprising the steps of:

(a) forming at least one patterned region atop a surface of an insulating region, said at least one patterned region comprising a Si-containing layer present atop said insulating region, a pad oxide present atop said Si-containing layer and a polish stop layer present atop said pad oxide;

(b) forming planarizing insulating regions abutting each patterned region, said planarizing insulating regions are formed on exposed portions of said insulating region, said planarizing insulating region being co-planar with a top surface of said polish stop layer;

(c) forming a hardmask on a portion of said at least one patterned region, said hardmask being used to define channel regions in said at least one patterned region;

(d) selectively removing a portion of said hardmask, said polish stop layer and said pad oxide layer so as to expose a portion of said Si-containing layer thereby forming channels regions and a trough;

(e) forming a gate region in said trough; and

(f) removing said polish stop layer and said pad oxide abutting said gate region so as to expose portions of said Si-containing layer and forming source/drain diffusion regions therein.

2. The method of Claim 1 wherein said Si-containing layer and said insulating region are components of a silicon-on-insulating (SOI) material.

3. The method of Claim 1 wherein step (a) comprising deposition, lithography and etching.

4. The method of Claim 1 wherein said planarizing insulating regions are formed by deposition and planarization.

5. The method of Claim 1 wherein said hardmask is formed by deposition of an oxide and patterning.

6. The method of Claim 1 wherein step (d) comprising a series of etching processes wherein various etchant gases or plasma are employed to selectively remove desired layers.

7. The method of Claim 1 wherein said gate region includes a gate dielectric, a gate conductor and insulating spacers.

8. The method of Claim 7 wherein said gate dielectric is formed by deposition or a thermal growing process.

9. The method of Claim 7 wherein said gate conductor is formed by deposition and planarization.

10. The method of Claim 7 wherein said gate conductor is comprised of polysilicon, amorphous silicon, a conductive elemental metal, a nitride or silicide of a conductive elemental metal, an alloy of a conductive elemental metal or multilayers thereof.

11. The method of Claim 7 wherein said insulating spacers are formed by deposition and etching.

12. The method of Claim 1 wherein said source/drain diffusion regions are formed by ion implantation and activation annealing.

13. A thin film insulating (FIN) metal oxide semiconductor field effect transistor (MOSFET) comprising:

a bottom Si-containing layer;

an insulating region present atop said bottom Si-containing layer, said insulating region having at least one partial opening therein;

a gate region formed in said partial opening, said gate region comprising two regions of gate conductor that are separated from channel regions by an insulating film, said insulating film having opposite vertical surfaces adjacent to the channel regions;

source/drain diffusion regions abutting said gate region, said source/drain diffusion regions having junctions that are self-aligned to the channels regions as well as the gate region; and

insulating spacers that separate the gate region and the source/drain diffusion region formed orthogonal to said insulating film.

14. The FIN MOSFET of Claim 13 wherein said insulating region includes an insulating layer of an SOI material.

15. The FIN MOSFET of Claim 13 wherein said partial opening exposes a portion of said insulating layer of said SOI material.

16. The FIN MOSFET of Claim 13 wherein said insulating film is formed surrounding a portion of a Si-containing layer, said insulating film is comprised of a gate dielectric.

17. The FIN MOSFET of Claim 16 wherein said gate dielectric is comprised of an oxide, a nitride, an oxynitride or any combination or multilayer thereof.

18. The FIN MOSFET of Claim 13 wherein said regions of gate conductor are each comprised of polysilicon, amorphous Si, a conductive elemental metal, an alloy of a conductive elemental metal, a nitride or silicide of a conductive elemental metal or multilayers thereof.

19. The FIN MOSFET of Claim 13 further comprising salicide regions formed atop said source/drain diffusion regions.

20. The FIN MOSFET of Claim 13 wherein said source/drain diffusion regions are formed in a portion of a patterned Si-containing layer.